including:

a plurality of the sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center.

Claim ~~11~~ 2 (three times amended). A semiconductor wafer, including:

a plurality of chip sections defined thereon by scribe lines, each chip section having:

bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center.